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HVDC Test-Bed Designing Using Matlab/Simulink

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Abstract: *Now a day's studies on HVDC circuit breaker (CB) prototypes have shown successful results. Effective and reliable solutions relating to massive fault energy during dc fault interruption have not yet commercialized, and dc current breaking topologies on ways of achieving artificial zero should be modified. As another, one possible solution is to mix fault current limiting technologies with dc breaking topologies. In this Research paper analysis about the applying of resistive superconducting fault current limiters (SFCLs) on various sorts of HVDC CB in order to estimate the consequences of combining fault current limiters and conventional dc breakers, and simulation is done using matlab software.*

Keywords: *SFCL, HVDC Circuit Breaker, Passive Resonance CB (PRCB), Inverse Current Injection CB, Hybrid HVDC CB.*

1. INTRODUCTION

In order to achieve commercial application of future Multi Terminal HVDC (MTDC) networks, typically considered an optimum solution for renewable energy transmission and power grid inter-connection, the reliability of HVDC systems must be guaranteed [1], [2]. Conventional point-to-point HVDC systems can be sufficiently protected via mechanical circuit breakers located on the AC side [3]; however, a selective coordination protection scheme that isolates faulted lines should be utilized in MTDC to prevent the blackout of the entire grid system [4]. HVDC circuit breakers (HVDC CB) are widely considered a key technology in the implementation of the MTDC system [5]. Generally, fault current interruption can be easily achieved via zero-current crossing. While AC circuit breakers can interrupt a fault current in natural zero current, artificial current zero should be implemented for DC breakers to enable fault current interruption. To fulfill the zero-crossing condition of DC fault current, a forced current reduction method should be implemented. Various type of HVDC CB are summarized [6], some of which have revealed prototypes and successful test results. An effective and reliable solution considering massive fault energy during DC fault interruption is still lacking. Existing DC current breaking topologies focusing solely on methods to achieve artificial current zero should be somewhat modified [7]. As an alternative, one feasible solution is to combine fault current limiting technologies with DC breaking topologies. In this work, we investigated application studies of resistive SFCL on the various types of HVDC CB in order to estimate the effects of combining fault current limiters and conventional DC breakers. Resistive SFCL have been acknowledged as an effective solution to effectively limit fault current levels by absorbing electrical and thermal energy stresses during fault [8]. In this light, the combined application of SFCL and HVDC CB could be an attractive alternative solution capable of drastically decreasing the dissipated fault energy and improving the performance of HVDC CBs. In order to estimate the performance of combined application of SFCL on HVDC CBs, simulation studies were performed using Matlab/Simulink.

2. Modeling of SFCL and HVDC Circuit Breakers

Four types of DC breakers and SFCL were modeled, and fault current interruption characteristics were compared to determine the HVDC CBs type most suitable for the application of SFCL considering the current interruption capability and reduction of total dissipated energy during DC fault.

2.1 HVDC Test-bed Model

In order to analyze the impact of SFCL on various types of HVDC CBs, a test-bed model was designed in Matlab /Simulink as illustrated in Fig.1 The simple, symmetrical, monopole, point-to-point, 2-level, half-bridge HVDC system was utilized to concentrate the interruption performance of the DC fault current in detail. The AC network adjacent to the HVDC link was substituted by equivalent RL impedance, which enabled the X/R ratio of the power system to be determined.

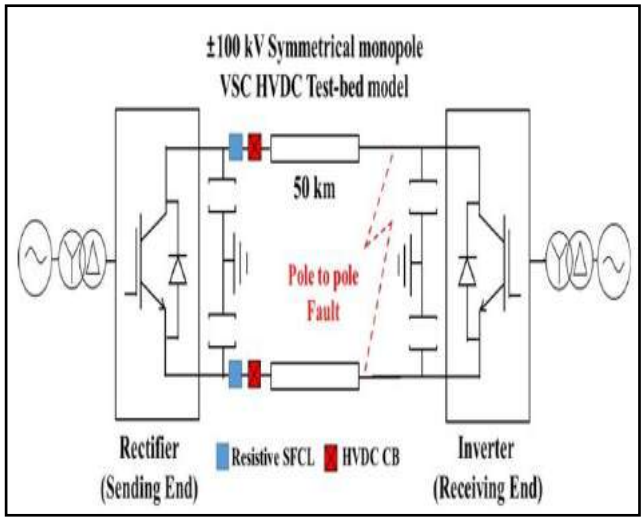

Fig -1: *level point-to-point HVDC test-bed model (V_{ac}: AC voltage, R_{ac}, Lac: system impedance of AC, L_p: Phase reactor)*

The converter transformer was a wye-delta connection. A phase reactor, L_p, was added between the converter and transformer to filter the harmonics during conversion. Each type of HVDC CB and SFCL was located at the output of the rectifier. Detailed specifications of the HVDC link are as follows: the rated voltage = ±100 kV, nominal current = 1 kA, nominal power flow = 100 MW, and the transmission line length = 50 km.

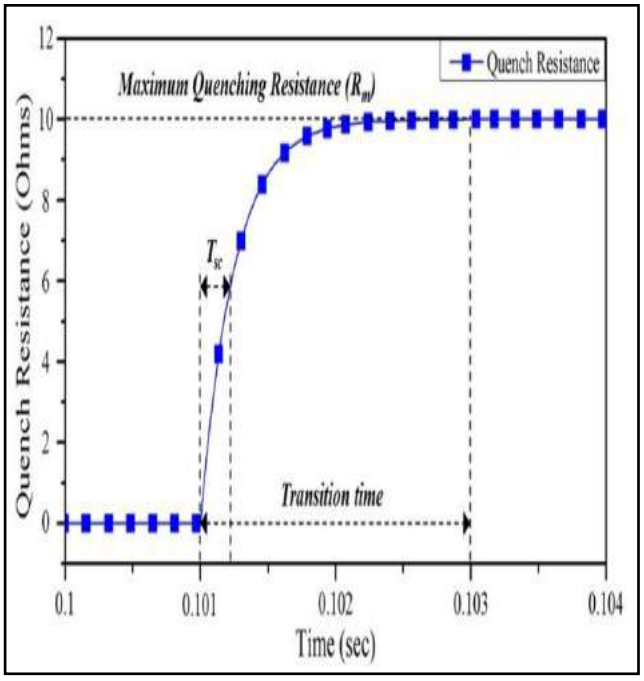

Fig -2: *Quenching characteristics of the designed resistive SFCL with time.*

2.2 Resistive Superconducting Fault Current Limiter

The resistive SFCL, which is based on the quenching phenomena of superconductors, has been an area of great interest for researchers in the last decade [9], and several prototypes have been developed and installed in medium- and high-voltage systems [10]. Focusing on the theoretical approaches for a resistive SFCL [11],the quenching phenomena of SFCL can be expressed as:

$$R_{SFCL}(t) = \begin{cases} 0 & (t < t_{quenching}) \\ R_m(1-\exp(-t/T_{sc})) & (t_{quenching} < t) \end{cases}$$

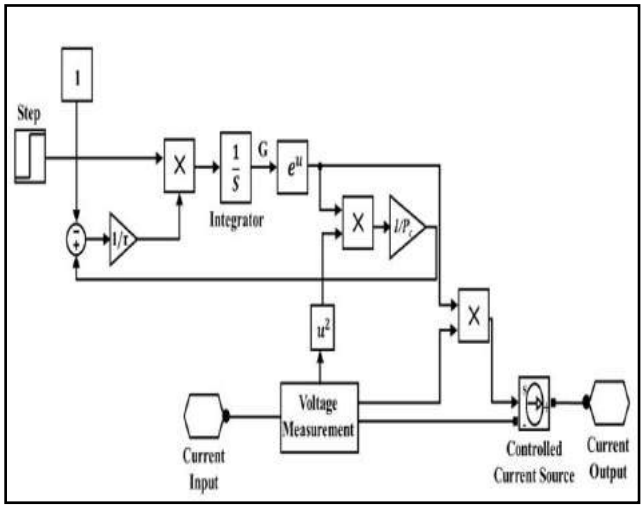

Fig -3: *The modified Mayr black-box arc model designed using Matlab/ Simulink for discrete simulation environment*

Where R_m is the maximum quenching resistance and TSC is the time constant for the transition to the quenching state. In this work, the SFCL rating was 100 kV DC with a 2 kA of critical current. The maximum quenching resistance, R_m, is 10 Ω. In order to acquire nearly 10 ohms of R_q within 2 ms, the value of T_{sc} was determined to 0.25 ms. the quenching characteristics of the designed SFCL based on above equation are shown in Fig. 2.

3. CASE STUDY

Transient fault simulations were conducted to analyze the effects of SFCL on various HVDC CB types. Each type of HVDC CB, both with and without SFCLs, was applied at the sending end of the test-bed.

A pole-to-pole fault, which considered a severe fault in HVDC systems, was generated on the receiving end at 0.1 sec. The prospective maximum fault current without any protection devices was 14.7 kA in the designed test-bed. The rising rate of the fault current di/dt during early 10 ms was measured as 589 A/ms. Therefore, considering high rising rate of the fault current, fast interruption should be achieved.

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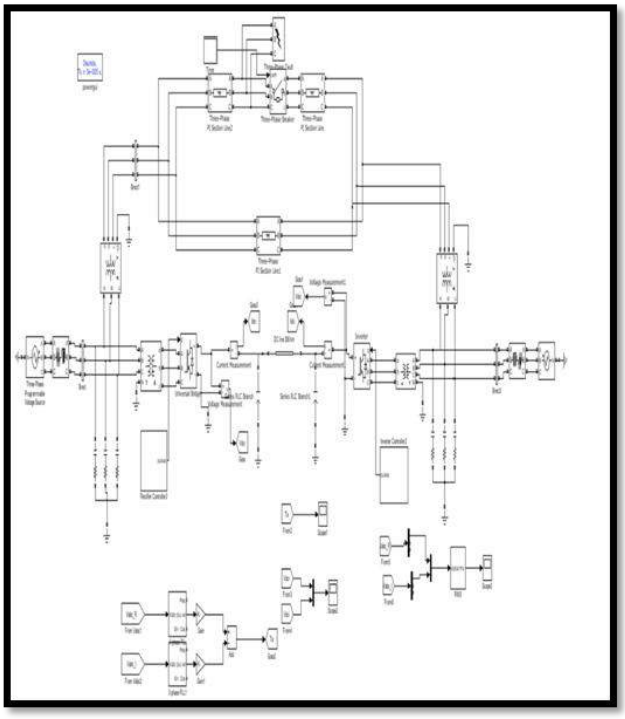

Fig -4: *Main Proposed System*

Generally, fault current interruption can be easily achieved via zero-current crossing. While AC circuit breakers can interrupt a fault current in natural zero current, artificial current zero should be implemented for DC breakers to enable fault current interruption.

To fulfill the zero-crossing condition of DC fault current, a forced current reduction method should be utilized, and various type of HVDC CB are summarized in [6], some of which have revealed prototypes and successful test results. Nevertheless, an effective and reliable solution considering massive fault energy during DC fault interruption is still lacking. Existing DC current breaking topologies focusing solely on methods to achieve artificial current zero should be somewhat modified [7]. As an alternative, one feasible solution is to combine fault current limiting technologies with DC breaking topologies.

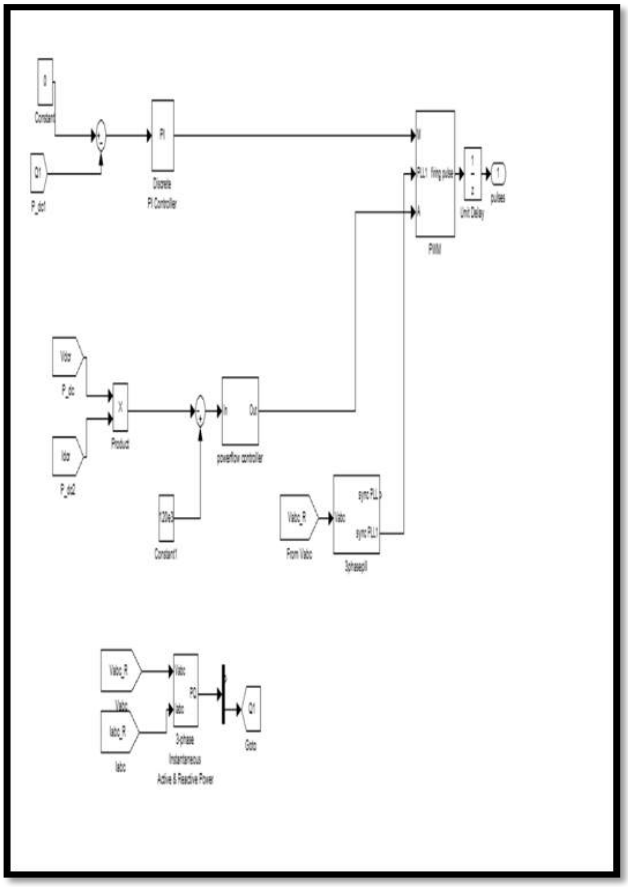

Fig -5: *Sending end Control subsystem*

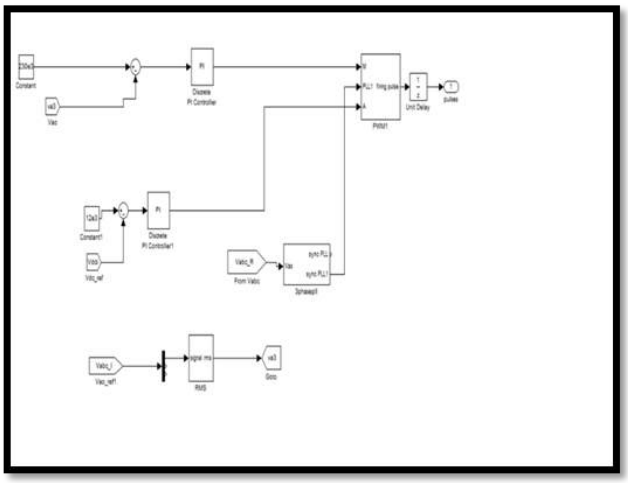

Fig -6: *Receiving end control subsystem*

In this work, we investigated application studies of resistive SFCL on the various types of HVDC CB in order to estimate the effects of combining fault current limiters and conventional DC breakers. Resistive SFCL have been acknowledged as an effective solution to effectively limit fault current levels by absorbing electrical and thermal energy stresses during fault [8]. In this light, the combined application of SFCL and HVDC CB could be an attractive alternative solution

capable of drastically decreasing the dissipated fault energy and improving the performance of HVDC CBs.

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4. SIMULATION RESULTS

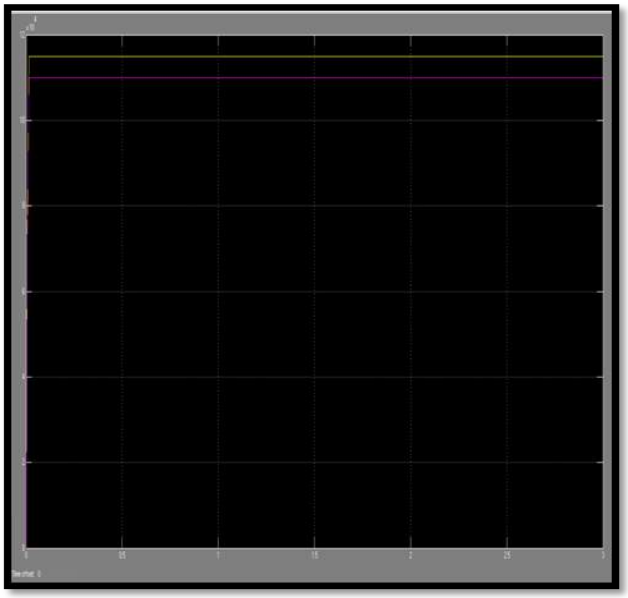

Fig -7: *Sending and Receiving end Controlled Voltage*

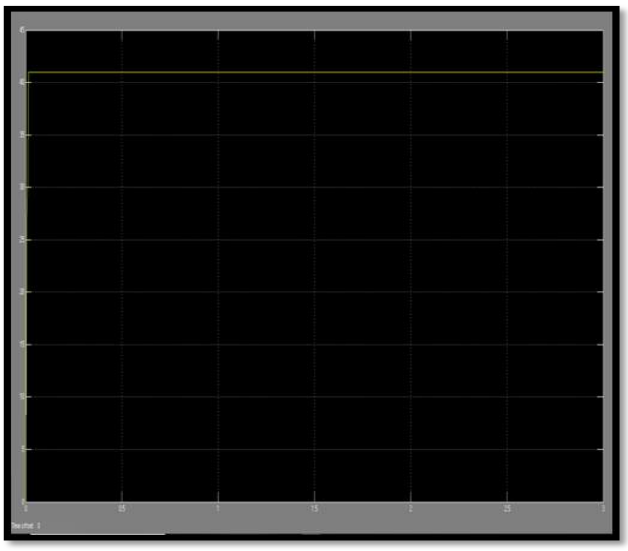

Fig -8: *Constant Angular Frequency*

5. CONCLUSION

This research paper deals with the impact of SFCL on various types of HVDC CB. The resistive SFCL considers quenching characteristics and concepts of HVDC CB models including the black-box arc model, and a simple HVDC test-bed were designed using Matlab/Simulink. A severe DC pole-to-pole fault was imposed to analyze the interruption performance. From the simulation results, the maximum fault current, interruption time, and dissipated energy stress on an HVDC CB could be decreased by applying an SFCL.

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