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# Modeling and Simulation of 13-level Cascaded Hybrid Multilevel Inverter with less number of Switches

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**Abstract:** *This paper presents the modeling and simulation of 13-level cascaded hybrid multilevel inverter (MLI) for with less number of switches. MLI is one of the most efficient power converters which are especially suited for high power applications with reduced harmonics. MLI not only achieves high output power and is also used in renewable energy sources such as photovoltaic, wind and fuel cells. This paper mainly focuses on cascaded MLI with three unequal DC sources called asymmetric cascaded MLI which reduces the number of power switches. The sinusoidal pulse width modulation (SPWM) is improves the output voltage at lower modulation index for obtaining lower Total Harmonic Distortion (THD) level. The gating signal for the 13-level hybrid inverter using SPWM technique is generated. This proposed modulation technique results in reduced percentage of THD, but lower order harmonics are not eliminated. So a new technique called Selective Harmonic Elimination (SHE) is also implemented in order to reduce the lower order harmonics. The performance evaluation of the proposed pulse width modulation (PWM) inverter is verified using 13-level cascaded hybrid MLI with MATLAB / Simulink model.*

**Keywords:** *Multilevel Inverter (MLI), Sinusoidal Pulse Width Modulation (SPWM), Selective Harmonic Elimination (SHE), Total Harmonic Distortion (THD).*

## 1. INTRODUCTION

The inverters are relied upon to give sinusoidal yields yet the viable inverters produce non-sinusoidal yield and subsequently contain harmonics. So to combine a close sinusoidal component and to lessen the harmonic distortion multilevel inverters have emerged. It is this creating innovation that has affected the battery packs in electric vehicles in light of the likelihood of high power rating without the utilization of transformer. Among the different multilevel structures that were introduced by researchers, the cascaded multilevel inverter turns out to be much predominant in harmonic reduction.

Further, the low order harmonic contents which are available can be minimized by exchanging switching strategies. Selective Harmonic Elimination Pulse Width Modulation (SHEPWM) technique was developed for multilevel converters to eliminate lower order harmonics. The trigonometric terms in the equations create multiple solutions thereby, making it complex to control the switching angle and hence reduce the lower order harmonics. The arithmetic solutions which are the switching angles of inverter suppress the lower order harmonics. Research was carried out to solve these equations by mathematical methods and evolutionary algorithms. Mathematical methods are derivative based and needs initial assumptions. Different topologies like diode-clamped inverter, capacitor-clamped, and cascaded multilevel inverter with separate DC sources were developed [1-5].

An optimal modulation technique [6] to reduce the switching losses was proposed, but this technique had more conduction losses due to high output currents and due to the series connection of several semiconductors. Despite the fact that different novel algorithms for Selective Harmonic Elimination were created [7-8], yet they slacked in the capacity to take out substantial number of low order harmonics. This lead to the advancements in selective harmonic elimination pulse width modulated technique based on the foraging behavior of a colony of ants [9]. This method has improved calculation, subordinate free operation, and achieves close optimal convergence. A generalized formulation for selective harmonic elimination pulse width modulation control suitable for high voltage, high power cascaded multilevel Voltage Source Converters (VSC) with both equivalent and non square with DC sources utilized as a part of constant frequency utility applications was produced in relationship with genetic algorithm [10-12].

 

In recent years multilevel inverter plays an important role and attracts more attention in the conversion of medium power applications. It is simple in construction, better-quality in performance and produces lesser harmonics. Also it has lower switching losses, high *dv/dt* rating and reduced switching stresses and harmonics. The three commercial topologies of multilevel voltage source inverters are (i) the Neutral Point Clamped (NPC) or diode clamped multilevel inverter (DCMLI), (ii) flying capacitor multilevel inverter (FCMLI) and (iii) cascaded H bridge (CHB) multilevel inverter. Unlike DCMLI and FCMLI the CMLI does not require voltage clamping diodes and voltage balancing capacitors. This paper focuses particularly on cascaded hybrid multilevel inverter [13-16] which requires independent DC sources i.e. for "*n*" number of DC sources the number of levels obtained will be *(2n + 1)*.

In view of DC source, the CHB multilevel inverter is further divided into two topologies namely symmetric and asymmetric inverters. The values of all the voltage sources are equal in symmetric topology. In symmetric topology if the number of output voltage levels is increased, it results in rapid increase in number of switching devices. So in order to increase the number of output voltage levels with less number of switching devices the different value of DC sources are selected which is named as asymmetric topology [17-18]. Among these two topologies, asymmetric cascaded MLI is explained in this paper and it requires three unequal DC sources to produce thirteen-level output. This new topology has been proposed to obtain 13-level output with minimum number of switches. In addition to that the THD are reduced and specified harmonics are eliminated using selective harmonic elimination pulse width modulation (SHE PWM) technique.

## 2. CASCADED MULTILEVEL INVERTER TOPOLOGY

Normally a CMLI requires "*n*" dc sources for (*2n + 1*) level. But it is difficult to use separate DC sources for many applications since it requires many long cables and could lead to voltage imbalance among the DC sources. Fig 1 represents CMLI consisting of two H-bridges. Each H-bridge is provided with separate different values of dc source as *Vdc* for bridge 1 and *Vdc/2* for bridge 2. The output of H-bridge 1 is denoted as $V_1(t)$ and another one as $V_2(t)$. If the number of levels is increased it results in increase in number of H-bridges.

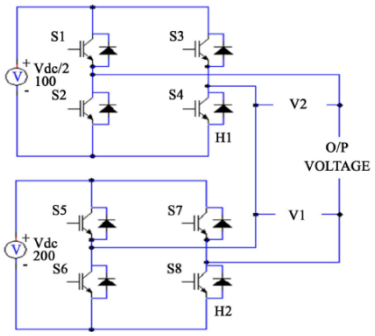


**Fig 1**: *CMLI with unequal dc sources*

The output phase voltage is given by Eqn. (1)

$$V_0(t) = V_1(t) + V_2(t) \quad (1)$$

The maximum output voltage is given by Eqn. (2)

$$V_{0max} = NV_{dc} \quad (2)$$

The inverters are relied upon to give sinusoidal yields yet the viable inverters produce non-sinusoidal yield and subsequently.

Fig 2 shows an 11 level inverter output $V_0(t)$. The major advantages of Cascaded Multilevel Inverter-Asymmetric-Topology are (i) less Number of dc sources; (ii) low switching losses; (iii) output switching frequencies are low; (iv) cost and complexity are reduced; (v) reduced harmonics level and (vi) increased output efficiency.

## 3. PROPOSED SELECTIVE HARMONIC ELIMINATION (SHE) PWM TECHNIQUE

In SPWM it has several carrier signals keeping only one modulating signal. The carrier signals are triangular one and have same frequency and peak to peak amplitude so that the bands they occupy are contiguous i.e. one carrier signal will have a contact with other signal. The modulating signal is pure sinusoidal and at every instant each carrier signal is compared with modulating signal. In each comparison if the modulating signal is greater than the carrier signal it gives one or otherwise zero. The results are added to give the voltage level, which is required at the output terminal of the inverter.

SHE is commonly adopted in medium and high power inverter applications where the switching frequency is low enough to minimize the switching losses. The effectiveness of this method is fully depends on switching angles. So, for determining the optimum switching angles several algorithms have been developed. Usually it is done using optimization techniques such as Newton Raphson method [19-20].

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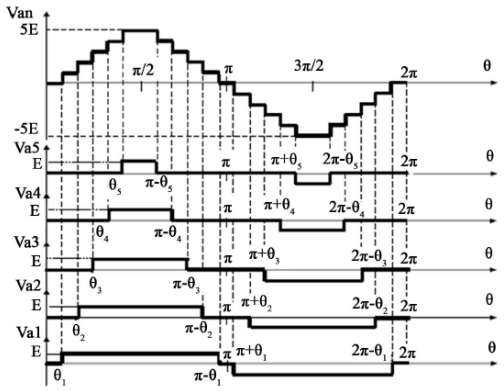


**Fig 2**: *A cascaded 11 level inverter output.*

The digital implementation of SHE equations involves two steps are (i) The switching angles are too calculated through a set of non-linear and transcendental equations. (ii) The determined switching angles are to be stored in look up table for real time applications. In this paper for finding the values of switching angles the Newton Raphson method has been implemented which has a set of solutions to reduce the lower order harmonics.

The main advantages of this SHE is to obtain lower order harmonics at the output side. If the inverter wants to supply AC power to an AC load with constant frequency a filter is usually installed in its output side. In this method when the lower order harmonics are eliminated the output will have only higher order harmonics and it should be attenuated by the filter. Hence the cut-off frequency will be increased which will results in filter size.

## 4. PROPOSED SINGLE PHASE CASCADED MULTILEVEL INVERTER - ASYMMETRIC TOPOLOGY

The new design of topology is required to form an asymmetric inverter as shown in Fig 3. The switching states and voltage levels of the proposed inverter are shown in Table 1.

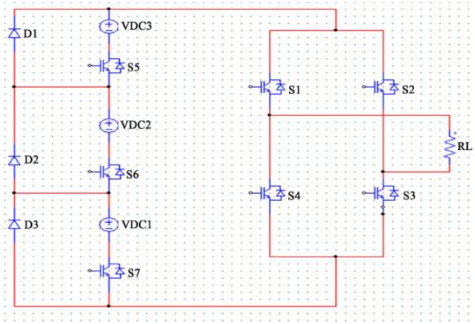


**Fig 3**: *Proposed circuit for Cascaded 13-level Inverter-Asymmetric Topology.*

**Table 1:** *Switching states and voltage levels of 13-level inverter.*

| *Switching States* | | | | | | | *Output Voltage* |
|---|---|---|---|---|---|---|---|
| *S1* | *S2* | *S3* | *S4* | *S5* | *S6* | *S7* | *(Vd)* |
| *1* | *0* | *1* | *0* | *0* | *0* | *1* | *+Vd* |
| *1* | *0* | *1* | *0* | *0* | *1* | *1* | *+Vd/6* |
| *1* | *0* | *1* | *0* | *0* | *1* | *1* | *+Vd/3* |
| *1* | *0* | *1* | *0* | *1* | *0* | *0* | *+3Vd/6* |
| *1* | *0* | *1* | *0* | *1* | *0* | *1* | *+2Vd/3* |
| *1* | *0* | *1* | *0* | *1* | *1* | *1* | *+4Vd/5* |
| *0* | *0* | *0* | *0* | *0* | *0* | *0* | *0* |
| *0* | *1* | *0* | *1* | *0* | *0* | *1* | *-Vd* |
| *0* | *1* | *0* | *1* | *0* | *1* | *1* | *-Vd/6* |
| *0* | *1* | *0* | *1* | *0* | *1* | *1* | *-Vd/3* |
| *0* | *1* | *0* | *1* | *1* | *0* | *0* | *-3Vd/6* |
| *0* | *1* | *0* | *1* | *1* | *0* | *1* | *-2Vd/3* |
| *0* | *1* | *0* | *1* | *1* | *1* | *1* | *-4Vd/5* |

Here there are 3 DC sources connected with seven switches which include an H-bridge inverter. All IGBT switches are connected as shown in the Fig 3 in order to form a hybrid cascaded inverter. The new topology comprises a control of modulation index level to form various levels of inverter. Three Flywheel diodes are used to prevent the back emf from triggering and other circuits in the proposed model. The gating signal for 13-level inverter is generated for employing the SPWM technique.

To produce a 13-level output the proposed modulation technique carries six carrier signals with one modulating signal. The carrier waveform for the proposed system is shown in Fig 4.

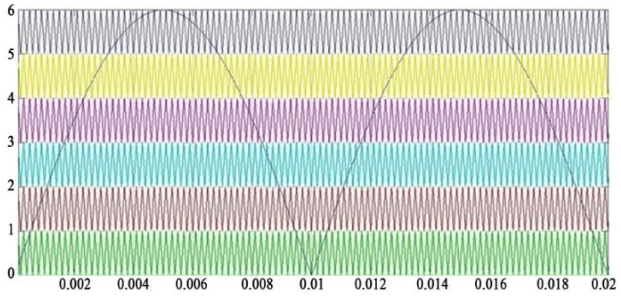


**Fig 4**: *Carrier waveform for SPWM technique.*

## 5. SIMULATION RESULTS AND DISCUSSION

By using MATLAB/Simulink the proposed 13-level inverter is simulated by using Insulated Gate Bipolar Transistor (IGBT) switches. Here only 7 switches are used to produce 13-level output along with 3 feedback diodes. The staircase output voltage and current waveform of 13-level inverter thus obtained is shown in Fig 5.

 

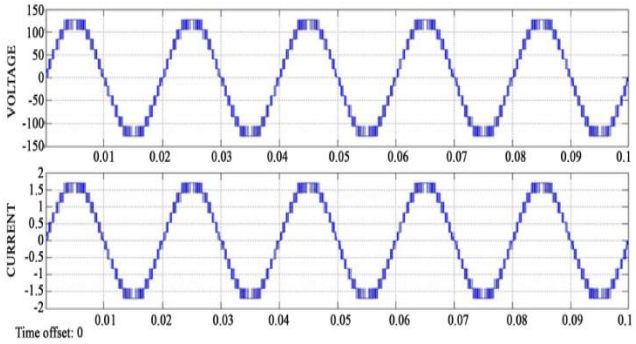


**Fig 5**: *Output voltage and current waveform.*

The staircase output and the FFT analysis for THD% is shown in Fig 6.

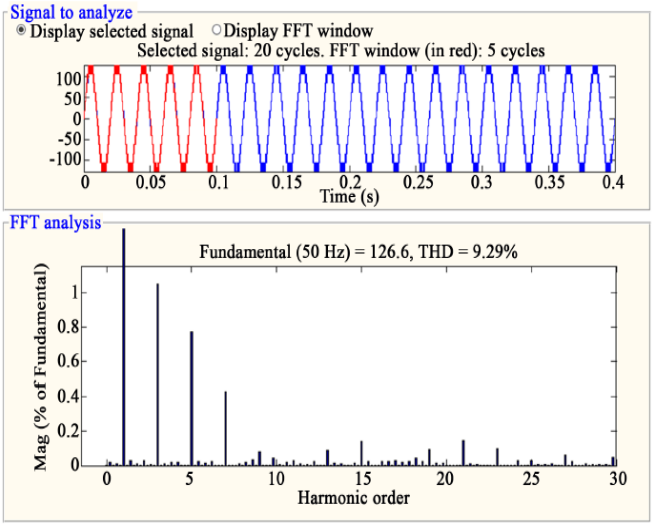


**Fig 6:** *FFT analysis for 13-level inverter with R load.*

From the obtained result the THD for R load is 9.29% at 1500 Hz frequency for 126.6 V. The simulation result that the odd harmonics of 3rd, 5th, 7th, and 9th harmonic levels are most dominant. Hence a new method of SHEPWM is suggested for minimizing such kind of odd harmonics.

The FFT analysis of 13-level inverter with R load for Mi = 0.97 using SHE technique is shown in Fig 7. By using SHE technique the 3rd, 5th, 7th, and 9th harmonics are minimized by varying the modulation index from 0 to 1.

For the modulation index 0.85, the switching angles are 0.62, 23.10, 44.42, 54.37 and 63.57 the THD is 8.59%. If the modulation index is 0.97 the various switching angles are 4.82, 12.69, 23.32, 24.46, 37.27 and THD is around 6.19% which highly satisfies the IEEE 519-1992 harmonic guidelines. Thus if the modulation index has been increased the % THD would be reduced.

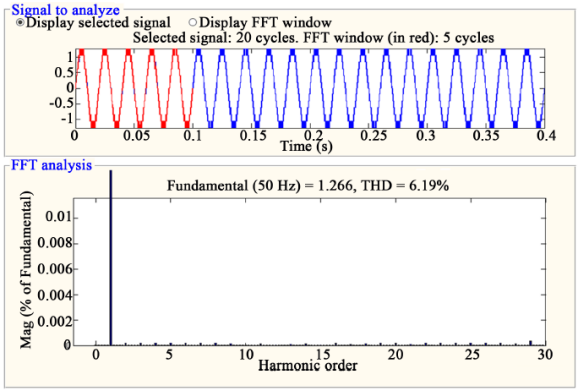


**Fig 7:** *FFT analysis of 13-level inverter with R load for Mi = 0.97 using SHE technique.*

## 6. CONCLUSION

The analysis of the modeling and simulation of 13-level cascaded hybrid multilevel inverter (MLI) for with less number of switches is implemented. The proposed topology of 13-level cascaded hybrid MLI is verified with the satisfied results of MATLAB/Simulink model. This topology is also simulated by using SHEPWM technique for minimizing the most dominant odd harmonics. The ratio (1:2:4) of the DC source voltage and the firing angle computation has performed to obtain a minimum THD value of the load voltage and current. Here the realization of the modulation index is also observed for maintaining the AC output voltage by varying the modulation index between $0 < m \leq 1$. From the above analysis by the comparison of output results, it is realized that the proposed model resulted lower THD level which could meet the IEEE 519-1992 standard.

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